14/Appeal Brief 7-27-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:

Rosenberg et al.

Serial No.: 08/993,104

Filed: December 18, 1997

For: VOLTAGE SIGNAL MODULATION SCHEME

Date: July 11, 2000

Art Unit: 2774

Examiner: F. Nguyen

HONORABLE DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Washington, D.C. 20231

APPEAL BRIEF

IN SUPPORT OF APPELLANTS' APPEAL

TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in triplicate in support of their Appeal from a final decision by the Examiner in the above-captioned case. Appellants respectfully request consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
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INTEL CORPORATION
Name of Assignee

Heather Adamson 7/12/00
SIGNATURE DATE

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-14 and 16-25 are currently pending in the above-referenced patent application. Claims 1-14 and 16-25 were rejected in the Final Office Action mailed on December 28, 1999 and are the subject of this appeal. The Examiner confirmed the final rejection in an Advisory Action mailed on May 5, 2000.

Claims 1-14, 16-20, 22, and 24-25 stand rejected under 35 U.S.C. 112, second paragraph, and claims 1-14 and 16-25 stand rejected under 35 U.S.C. § 103(a) over U.S. patent 5,436,635 by Takahara et al. in view of U.S. Patent 4,870,396 by Shields.

IV. STATUS OF AMENDMENTS

To the best of Appellants' knowledge, no amendments have been filed subsequent to the Final Rejection.

A copy of all claims on appeal, namely claims 1-14 and 16-25, is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

It is typical for liquid crystal displays, such as nematic liquid crystal cells including nematic liquid crystal material, to employ an AC voltage signal driven across the liquid crystal display light modulating elements in order to maintain a substantially zero DC bias. Without this, ionization and eventual degradation of the liquid crystal material may result.

FIG. 4 is a circuit diagram illustrating an embodiment 500 of a prior art active matrix pixel circuit. As illustrated, a transistor 510 is provided to address the particular pixel and a voltage to be applied to capacitor 520 is applied to the source of transistor 510. Transistor 510 is employed to maintain an alternating differential voltage across the liquid crystal material of the cell by driving alternating inverted voltages onto capacitor 520.

A disadvantage of this approach is the bandwidth to provide the desired AC voltage signal across the liquid crystal cell or material. In this embodiment, a voltage signal having an inverted polarity is applied to transistor 510 to replace the previous voltage signal applied. Therefore, for a sufficient number of pixels, such as one to two million, and a reasonable frequency, such as 40 to 60 hertz, a significant bandwidth is difficult to achieve in digital circuitry without introducing greater expense and/or complexity. Particular embodiments of Appellants' invention are intended to address these issues.

Simply stated, Appellants' claimed invention includes, as just one embodiment:

1. A circuit (e.g., circuit of FIG. 1) for modulating voltage signals comprising:

a first circuit configuration (e.g., transistors 130 and 140) to substantially simultaneously (e.g. transistors 130 and 140 are operating approximately at the same time) and asynchronously (e.g. transistors 130 and 140 are operating independently of activity occurring with other cells) drive respective positive and negative voltage signals onto respective voltage signal storage elements (e.g., storage capacitors 150 and 160);

and a second circuit configuration (e.g., transistors 115 and 190) to alternatively sample the respective voltage signals of the respective voltage signal storage elements (e.g., storage capacitors 150 and 160) at a substantially predetermined rate (e.g., a square wave signal).

More particularly, FIG. 1 is a circuit diagram illustrating an embodiment of a voltage signal storage circuit in accordance with the present invention. As illustrated, a digital-to-analog (DIA) converter 110 receives as an input signal, video data signals. As illustrated, DIA converter 110 produces analog voltage signals that are applied to differential amplifier 120. Differential amplifier 120 amplifies these analog voltage signals, and these amplified voltage signals are applied to transistors 130 and 140, as illustrated. Likewise, this particular cell is enabled by a cell enabler or cell select signal, CELL SELECT, which is applied to the gates of transistors 130 and 140. Therefore, when a signal is applied to the gates of transistors 130 and 140, the output voltage signal of differential amplifier 120 is stored on voltage signal storage elements, such as storage capacitors 150 and 160 here.

Transistors 190 and 115 are coupled in a configuration to operate as a multiplexer or MUX. Therefore, in this embodiment, a square wave signal and its complement may be respectively applied to the gates of transistors 190 and 115. By applying the square wave signals, in the configuration illustrated in FIG. 1, an alternating voltage is effectively applied across liquid crystal cell 125 at a substantially predetermined frequency.

Therefore, particular embodiments of the present invention may provide a circuit that may:

1) Apply a voltage potential to one storage element while <u>SUBSTANTIALLY SIMULTANEOUSLY</u> applying another voltage potential to a second storage element.

As stated on page 6, lines 9-32, transistors 130 and 140 may be enabled substantially simultaneously so that voltage potentials may be stored on storage elements 150 and 160. In the particular embodiment shown in FIG. 1, the gate of transistors 130 and 140 receive the same enable signal, CELL SELECT. As a result, transistors 130 and 140 may be enabled or turned on at substantially the same time. Thus, the voltage potentials may be stored onto the repsective storage elements at substantially the same time.

Accordingly, the circuit shown in FIG. 1 allows a positive voltage potential to be stored on one of the storage elements (e.g., storage elements 150 or 160), while a negative voltage potential is substantially simultaneously stored on the other storage element. Of course, one skilled in the art would understand that the voltage potentials may not be stored at exactly the same time due to a variety of reasons.

2) <u>ASNCHROUNOUSLY</u> drive voltage potentials onto the storage elements.

As stated on page 6, line 32, through page 7, line 5, of Appellants' specification, the circuit shown in FIG. 1, may apply the voltage signals to the respective capacitors or voltage signal storage elements asynchronously and arbitrarily. For example, the voltage potentials may be stored on storage elements 150 and 160 independently with respect to the application of other voltage signals to other voltage signal storage elements. Thus, voltage potentials may be driven onto storage elements 150 and 160 independently of other activity within the integrated circuit and asynchronously with respect to when other cells within an LCD system are updated or accessed. Moreover, voltage potentials may be driven onto storage elements 150 and 160 independently or asynchronously with respect to when the previous voltage potentials were applied.

An embodiment of a voltage signal modulation circuit in accordance with the present invention may provide several possible advantages. For example, as alluded to above, a lower bandwidth may be employed, such as for a liquid crystal display, and yet still achieve an image having a desired number of pixels. Likewise, if a voltage signal modulation circuit in accordance with the present invention, multiple image sources employing different frame rates may be combined without employing circuitry to synchronize the signals from the different sources. For example, because voltage signals are continually sampled from the storage capacitors, where multiple image sources are employed or combined, these signals may be rendered at their own individual frame rate since, to the end user, the visual changes occur asynchronously as the voltage signals are applied to the storage elements.

VI. ISSUES PRESENTED

A. Whether claims 1-14, 16-20, 22, and 24-25 are unpatentable under 35 U.S.C. § 112, second paragraph.

1. The Examiner has improperly relied on extrinsic evidence, and thus, has not established the requisite prima facie showing.
2. The intrinsic evidence (e.g., Appellants' specification) provides a clear and unambiguous meaning to the terms used in the claims.
3. The term "substantially" does not render a claim indefinite or vague.

B. Whether claims 1-14 and 16-25 are unpatentable under 35 U.S.C. 103(a) over U.S. patent 5,436,635 by Takahara et al. in view of U.S. Patent 4,870,396 by Shields.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1-14 and 16-25 stand or fall together as Group I.

VIII. ARGUMENT

A. REJECTION OF CLAIMS 1-14 AND 16-25 (GROUP I) UNDER 35 U.S.C. § 112, SECOND PARAGRAPH, IS IMPROPER.

1. THE FINAL OFFICE ACTION HAS IGNORED THE INTRINSIC EVIDENCE OF RECORD AND IMPROPERLY RELIED ON EXTRINSIC EVIDENCE TO REJECT CLAIMS 1-14 AND 16-25.

It is well settled that, in interpreting a claim, one should first look to the intrinsic evidence of record, i.e., the patent itself including the claims, the specification, and the prosecution history. Such **intrinsic evidence is the most significant source of the legally operative meaning of claim language**. *Markman v. Westview instruments Inc.* 52 F.3d 967, 979 (Fed. Cir. 1995) (emphasis added). Thus, the specification is always highly relevant to the claim analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term. *Vitronics Corporation v. Conceptronic Inc.* 90 F.3d. 1576, 1582 (Fed. Cir. 1996).

In contrast, extrinsic evidence is that evidence which is external to the patent and file history, such as expert testimony, inventor testimony, **dictionaries**, and technical treatises and articles. *Id.* at 1584. The *Vitronics* court held that **reliance on any extrinsic is improper** when the public record (i.e., patent specification) provides meaning for the claim language. *Id.* at 1582 (emphasis added). "Only if there were still some genuine ambiguity in the claims after consideration of all available intrinsic evidence..." should extrinsic evidence be used. *Id.* at 1584.

In rejecting claims 1-14 and 16-25, the Examiner merely quoted the claim language "substantially simultaneously and asynchronously" and then relied solely on the definition provided by Merriam-Webster's dictionary as the basis of the rejection. The Final Office Action stated:

> "According to Merriam-Webster's Collegiate Dictionary",
> simultaneously **means existing or occurring at the same time** (page 1094)

and asynchronously **means not happening, existing or arising at precisely the same time** (pages 72 and 1196)." (emphasis in original)

Appellants respectfully submit that the Examiner's reliance on the dictionary (extrinsic evidence) in this situation is not permitted under the law. Before extrinsic evidence may be used to interpret claim language, the Examiner is required by law to exhaust all possible sources of intrinsic evidence; in this case, Appellants' specification. As explained in more detail below, Appellants' specification includes several examples of the use of "simultaneously" and "asynchronously," both independently and together, that provide clear meaning for these terms as they are used in the claims. In actuality, Appellants would like to kindly point out that Appellants' application comprises at least 49 occurrences of the terms "simultaneously" or "asynchronously" that make the use of these terms clear.

Accordingly, extrinsic evidence, such as a dictionary, may only be considered if the Examiner has demonstrated that Appellants' specification, by itself, creates some **genuine ambiguity in the claims**. In other words, the Examiner must first establish at least a prima facie showing that the intrinsic evidence creates a genuine ambiguity in the claim language before the Examiner may rely upon extrinsic evidence to reject the claims.

In this case, the Examiner relied only on extrinsic evidence to reject claims 1-14 and 16-25. More importantly, the Examiner did not provide any explanation of how Appellants' specification, by itself, creates a genuine ambiguity in the language used in the claims. For example, the Examiner only admitted that Appellants' disclosure uses the terms "substantially simultaneously" and "asynchronously." (Final Office action, page 3, line 3). However, the Examiner simply stated that the use of the terms was not "clear cut." *Id.* By itself, the Examiner's statement that the use of these terms in the specification is not "clear cut" is not sufficient to establish that there is a genuine ambiguity in the claims.

More significantly, the Examiner did not provide any explanation of how the repeated uses of these terms, independent of any extrinsic evidence, creates a genuine ambiguity. The Examiner's unsubstantiated accusation that the use of the terms was not "clear cut" is not sufficient to establish that Appellants' specification creates a genuine

ambiguity. Therefore, the Examiner may not use extrinsic evidence to interpret the claims. **Appellants respectfully submit that the Examiner's reliance upon the dictionary is not only improper, but is also not relevant to interpreting the claims.** Until the Examiner establishes that the intrinsic evidence creates a genuine ambiguity, reliance upon extrinsic evidence is prohibited.

Accordingly, Appellants respectfully submit that the use of Merriam-Webster's dictionary is improper and the Examiner's comments based on the definitions provided by the dictionary may not be given any weight as a matter of law. *Vitronics* at 1583. Furthermore, Appellants would like to note that in rejecting claims 1-14 and 16-25, the Examiner relied solely upon the extrinsic evidence as the basis for rejecting claims 1-14 and 16-25. **Since the Examiner's comments relying on extrinsic evidence must be ignored, as a matter of law, the Examiner has not provided any explanation as to why claims 1-14 and 16-25 are vague or indefinite when in view of the specification.**

Because the extrinsic evidence must be ignored, the Examiner has failed to establish the requisite prima facie showing to reject claims 1-14 and 16-25 under 35 U.S.C. 112, second paragraph. Accordingly, the rejection is improper and Appellants respectfully request that the Board withdraw this rejection.

2. THE INTRINSIC EVIDENCE PROVIDES CLEAR AND UNAMBIGUOUS MEANINGS FOR THE TERMS USED IN CLAIMS 1-14 AND 16-25.

With respect to claims 1-14 and 16-25, the Final Office Action objected to the use of "substantially simultaneously and asynchronously" on the basis that the terms make the claims vague and indefinite. As explained above, the Examiner has failed to establish a prima facie showing that the claims are indefinite because the Examiner has improperly relied upon inadmissible extrinsic evidence. Thus, the burden has not shifted to Appellants to demonstrate that the claims are definite.

Nonetheless, in the interest of advancing the prosecution of this application and without conceding that a prima facie showing has been made, Appellants would like to demonstrate that the intrinsic evidence (e.g., Appellants specification) does not contain any ambiguities.

Appellants' specification makes the terms clear and unambiguous.

Appellants' specification comprises at least 49 occurrences of the terms "simultaneously" or "asynchronously," either independently from the other or together. Appellants respectfully submit that one skilled in the art would have a clear and unambiguous understanding of the claimed invention upon reading Appellants' specification. For the Board's convenience, Appellants' repeat claim 1 with reference to a particular embodiment of Appellants' invention as provided by Appellants' specification:

Claim 1. A circuit (e.g., circuit of FIG. 1) for modulating voltage signals comprising:

a first circuit configuration (e.g., transistors 130 and 140) to substantially simultaneously (e.g. transistors 130 and 140 operating approximately at the same time) and asynchronously (e.g. transistors 130 and 140 operating independently of activity occurring with other cells) drive respective positive and negative voltage signals onto respective voltage signal storage elements (e.g., storage capacitors 150 and 160);

and a second circuit configuration (e.g., transistors 115 and 190) to alternatively sample the respective voltage signals of the respective voltage signal storage elements (e.g., storage capacitors 150 and 160) at a substantially predetermined rate (e.g., a square wave signal).

1) Apply a voltage potential to one storage element while <u>SUBSTANTIALLY SIMULTANEOUSLY</u> applying another voltage potential to a second storage element.

Appellants' specification on page 2, lines 18-25, identifies one problem associated with conventional liquid crystal displays. Simply stated, an LCD display that has a large number of individual pixels to be charged may involve a high data rate. For example, two million pixels times 60 hertz times 8 bits per pixel may involve a data rate of 960 megabits per second.

As shown in FIG. 1, the gates of transistors 130 and 140 may be adapted to receive the same enable signal, CELL SELECT. In this particular embodiment, the CELL SELECT signal may be used to turn on transistors 130 and 140 at about the same time. When a signal is applied to the gates of transistors 130 and 140, "the output voltage signal of differential amplifier 120 is stored on voltage storage elements, such as storage capacitors 150 and 160 here" (see page 6, lines 14-16 of Appellants' specification).

Thus, in one embodiment of Appellants' invention, **"a first voltage potential signal value is applied or driven onto one ... voltage signal storage element, while substantially simultaneously, a second voltage signal value, comprising the logical inverse of that first voltage signal value, is applied or driven onto the other capacitor."** (see page 6, lines 28-

31 of Appellants' specification) (emphasis added). By charging two capacitors substantially simultaneously, the date rate of the LCD may be improved.

Accordingly, one skilled in the art would have a clear and unambiguous understanding of the term "substantially simultaneously" as used in claim 1 when read in view of the teachings of Appellants' specification.

2) <u>ASNCHROUNOUSLY</u> drive voltage potentials onto the storage elements.

Separately from the "simultaneous" feature of particular embodiments of Appellants' invention, Appellants' specification also describes particular embodiments of the invention where voltage signals are applied asynchronously to the storage elements. Although the scope of Appellants' invention is not limited in this respect, "... if a voltage signal modulation circuit in accordance with the present invention ... is employed, multiple image sources employing different frame rates may be **combined without employing circuitry to synchronize the signals from the different sources.** For example, because voltage signals are continually sampled from the storage capacitors, where multiple image sources are employed or combined, these signals may be rendered at their own individual frame rate since, to the user, **the visual changes occur asynchronously as the voltage signals are applied to the storage elements**" (see Appellants' specification page 7, lines 24-31).

Appellants' specification further states: "[a]lthough this feature has a number of associated advantages, one particular advantage is that it **enables asynchronous update to the light modulating element of the display.**" (page 7, lines 17-19). Thus, Appellants' specification clearly and unambiguously explains how a voltage potential may be driven to some storage elements of an LCD display independently of activity occurring with other storage elements. The voltage potentials may be driven onto storage elements independently of activity occurring on other storage elements, a voltage potential may be driven to a storage element asynchronously with respect to when the previous voltage potential was driven. For example, the voltage potential need not be driven at a fixed, synchronized rate, but rather, asynchronously. Thus, Appellants' specification makes clear how voltage signals may be driven onto storage elements asynchronously of other

activity. Accordingly, one skilled in the art would have a clear understanding of the use of "asynchronously."

The Final Office Action improperly treated these features as synonyms

Appellants believe that the Examiner may have improperly interpreted "simultaneously" and "asynchronously" as being complimentary to the same feature. The Examiner has apparently concluded that these terms were meant to be synonyms. Relying on this incorrect assumption, the Examiner then may have concluded that the terms are in conflict with each other. For example, the Final Office Action stated "[I]t is suggested that the claims are specifically directed to structural means as shown in the drawing to illustrate the combined simultaneously-asynchronously feature (see Final Office Action page 8).

However, Appellants respectfully submit that Final Office Action has improperly interpreted and combined these features. As demonstrated above, "simultaneously" and asynchronously" are two distinct features of particular embodiments of the disclosed invention.

As pointed out in the Final Office Action on page 3, the terms "substantially" and asynchronously" are used together on page 8, lines 15-18 of Appellants' specification. However, as demonstrated above, Appellants' specification includes many references that make clear that these are two different features. In addition, Appellants would like to point out that the terms "simultaneously" and "asynchronously" are often used in Appellants' specification separately from the other term. This further suggests that the terms refer to different features and it is improper to conclude they are synonyms.

Accordingly, Appellants respectfully submit that claims 1-14 and 16-25, when read in view of Appellants' specification, are clear and unambiguous.

3. THE USE OF "SUBSTANTIALLY" DOES NOT RENDER THE CLAIMS VAGUE OR INDEFINITE.

The Final Office Action also objected to the use of "substantially predetermined frequency" in claims 1-14 and 16-25. Appellants respectfully submit that Appellants' specification would reasonably apprise one skilled in the art of both the utilization and scope of this term as well.

Federal Courts and M.P.E.P. permit the use of "Substantially"

It is well settled that if the claims, read in light of the specification, reasonably apprise those skilled in the art both of the utilization and scope of the invention, and if the language is as precise and the subject matter permits, the courts can demand no more. (See, *Georgia-Pacific Corp. v. United States Plywood Corp.*, 258 F.2d 124,136 (2d Cir.).

More importantly, Courts have recognized that the use of "substantially" in a claim does not render the claim indefinite. The Court in *U.S. Philips Corp. v. National Micronetics Inc.* stated: "Although the statute requires an exact description of the invention, it does not require description in terms of exact measurement. All that is required is that the claims, when read in light of the specifications, inform those skilled in the art how to practice the invention and how infringement may be avoided. 188 U.S.P.Q. 662.

In Micronetics, the court considered whether "substantially equal" was indefinite. The court clearly found the term to permissible and definite in view of the specification. The Court held:

"The Court finds that the term "substantially equal" as used in each claim of the patent is not so indefinite as to render the patent invalid."

M.P.E.P. § 2173.05(b) also recognizes that the use of "substantially" is permitted and does not render a claim indefinite. It is well established that the term "substantially" simply implies that the condition need not exactly exist in order to fall within the scope of the claim. In the case of "substantially" equal, it is clear that the scope of the claim is not limited to situations requiring features to be "exactly" equal. Rather, it is understood that

the scope of the claim would include situations that are nearly equal due to variations expected by those skilled in the art.

With regard to claim 1, Appellants would like to kindly point out that page 9, lines 11-2214 of Appellants' specification states:

"Likewise, the sampling may **be alternatively at a substantially predetermined rate, so as, for example, to maintain a substantially zero bias,** although again the invention is not limited in scope in this respect." **(emphasis added)**

Accordingly, Appellants respectively submit that one skilled in the art would understand that the scope of the invention is not limited to situations where the frequency is exactly equal to the predetermined frequency. Rather, one skilled in the art would understand that the scope of the claims includes situations were the frequency is nearly or "substantially" equal to the predetermined frequency.

Appellants' would also like to point out that in order to properly reject a claim under 35 U.S.C. §112, second paragraph, the Examiner must first establish that the claim language raises a genuine ambiguity in the claim. In this case, the Examiner simply asserted that the term is indefinite without providing any explanation supporting why the term creates ambiguity. Accordingly, Appellants respectfully submit that the Examiner has not established a prima facie showing that the use of "substantially predetermined frequency" is vague and indefinite. Moreover, Appellants respectfully submit that one skilled in the art would understand the scope of the claims, when read in light of the specification.

Accordingly, Appellants respectfully request that the Board over turn the rejection of claims 1-14 and 16-25 under 35 U.S.C. § 112, second paragraph.

B. REJECTION OF CLAIMS 1-14 AND 16-25 (GROUP I) UNDER 35 U.S.C. § 103(a) IS IMPROPER.

The Final Office Action also rejects claims 1-14 and 16-25 under 35 U.S.C. §103(a) as being unpatentable over Takahara et al. (US Patent 5,436,635) in view of Shields (US Patent 4,870,396). Appellants respectfully traverse this rejection in view of the remarks that follow.

THE EXAMINER HAS NOT ESTABLISHED A PRIMA FACIE SHOWING OF OBVIOUSNESS.

It is well established that a prima facie showing of obviousness requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142). Without conceding the appropriateness of the combination, Appellants respectfully submit that the rejection is improper because the Examiner has not established a prima facie showing of obviousness of all the elements of independent claims 1, 9, 14, 18, 22, and 24.

With regard to independent claims 1, 9, 18, and 24, Appellants would like to kindly point out that each of these independent claims recites a circuit or circuit configuration to "substantially and asynchronously" drive respective voltage signals. Similarly, claims 14 and 22 recite the step of applying signals "substantially simultaneously and asynchronously."

However, the Examiner has ignored at least the "asynchronous" feature of the claims. As admitted in the Final Office Action "... the claims are specifically directed to structural means as shown in the drawings to illustrate the combined simultaneously-asynchronously frequency." Rather the Examiner chose to ignore these terms because they were considered by the Examiner to make the claims vague and indefinite. As explained above, these terms are clear and unambiguous, and thus, may not be ignored by the examiner.

More significantly, the Examiner did not provide any explanation as to how either Takahara et al or Shields asynchronously drives voltage potentials onto storage elements. Thus, Appellants respectfully submit that the Final Office Action did not provide any

explanation how the combination of Takahara et al. and Shields anticipate the "simultaneous **and** asynchronous" feature of the claims. Consequently, Appellants is left to speculate as to how the combination of Takahara et al. and Shields makes this feature of the claimed invention obvious.

However, Appellants would like to kindly point out that the burden to rebut and showing of obviousness does not shift to Appellants until a prima facie showing of obviousness has been established. Since the Examiner did not provide any explanation as to how the combination makes all the features and limitations of claims 1, 9, 14, 18, 22, and 24 obvious, the Examiner has not established a prima facie showing of obviousness, and thus, the rejection is improper.

Since claims 2-8, 10-13, 16-17, 19-21, 23, and 25 depend from these claims, the Final Office Action has not established a prima facie showing of obviousness of these claims as well.

IX. CONCLUSION

Appellants respectfully submit that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $300.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to Deposit Account No. 02-2666.

Respectfully submitted,

Date: 7-11-00

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X. APPENDIX A: CLAIMS ON APPEAL

1 A circuit for modulating voltage signals comprising:

a first circuit configuration to substantially simultaneously and asynchronously drive respective positive and negative voltage signals onto respective voltage signal storage elements;

and a second circuit configuration to alternatively sample the respective voltage signals of the respective voltage signal storage elements at a substantially predetermined rate.

2 The circuit of claim 1, and further comprising a liquid crystal cell coupled to said second circuit configuration.

3 The circuit of claim 2, wherein the substantially predetermined rate is related, at least in part, to the particular liquid crystal material of the liquid crystal cell.

4 The circuit of claim 2, wherein said first circuit configuration includes circuitry to address said liquid crystal cell.

5 The circuit of claim 4, wherein said circuit for modulating voltage signals is coupled in a liquid crystal display (LCD) system;

said LCD system being adapted to substantially simultaneously and asynchronously drive additional voltage signals onto respective voltage signal storage elements so that the stored voltage signals of the respective voltage signal storage elements are refreshed.

6 The circuit of claim 2, wherein said second circuit comprises a plurality of transistors coupled to electrically isolate said voltage signal storage elements from said liquid crystal cell while alternatively sampling the respective voltage signals of the respective voltage signal storage elements.

7 The circuit of claim 1, wherein the voltage signal storage elements comprise capacitors.

8 The circuit of claim 1, wherein said circuit for modulating voltage signals is embodied on an integrated circuit chip.

9 A liquid crystal display (LCD) system comprising:

a voltage signal modulation circuit to locally modulate the voltage signal applied across a liquid crystal cell in said LCD system;

said voltage signal modulation circuit including a first circuit configuration to substantially simultaneously and asynchronously drive respective positive and negative voltage signals onto respective voltage signal storage elements and a second circuit

configuration to alternatively sample the respective voltage signals of the respective voltage signal storage elements at a substantially predetermined rate.

10 The LCD system of claim 9, and further comprising at least one liquid crystal cell coupled to said voltage signal modulation circuit.

11 The LCD system of claim 10, wherein the substantially predetermined rate is related, at least in part, to the particular liquid crystal material of the liquid crystal cell.

12 The LCD system of claim 10, wherein said system includes circuitry to address said at least one liquid crystal cell.

13 The LCD system of claim 10, wherein said LCD system is adapted to substantially simultaneously and asynchronously drive additional voltage signals onto the respective voltage signal storage elements so as to refresh the stored voltage signals.

14 A method of modulating a voltage signal locally comprising:

applying respective positive and negative voltage signals to respective voltage signal storage elements substantially simultaneously and asynchronously; and

sampling the voltage signals of the respective voltage storage elements alternatively at a substantially predetermined rate.

16 The method of claim 15, wherein the substantially predetermined rate is related, at least in part, to the particular liquid crystal cell material of the liquid crystal cell.

17 The method of claim 14, wherein the voltage signal storage elements comprise capacitors.

18 A voltage signal modulation circuit comprising:

a first circuit to substantially simultaneously and asynchronously drive respective voltage signals onto respective voltage signal storage elements; and

a second circuit to sample the voltage signals of the respective voltage signal storage elements so as to locally produce a modulated voltage signal.

19 The voltage signal modulation circuit of claim 18, wherein the voltage signals comprise respective positive and negative voltage signals and the respective voltage signal storage elements comprise two respective voltage signal storage elements;

said first circuit being adapted to substantially simultaneously and asynchronously drive the respective positive and negative voltage signals onto the two respective voltage signal storage elements.

20 The voltage signal modulation circuit of claim 18, wherein said second circuit is adapted to sample the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate.

21 The circuit of claim 18, wherein said second circuit is further adapted to sample the voltage signals of the respective voltage signal storage elements so as to substantially maintain a substantially DC bias.

22 A method of modulating a voltage signal locally comprising:

applying respective voltage signals to respective voltage signal storage elements substantially simultaneously and asynchronously; and

sampling the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate so as to locally produce the modulated voltage signal.

23 The method of claim 22, wherein the voltage signals of the respective voltage signal storage elements are sampled so as to substantially maintain a substantially DC bias.

24 A display system comprising:

a voltage signal modulation circuit to locally modulate the voltage signal applied across a light modulating element in said display system;

said voltage signal modulation circuit including a first circuit configuration to substantially simultaneously and asynchronously drive respective voltage signals onto respective voltage signal storage elements and a second circuit configuration to sample the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate so as to locally produce a modulated voltage signal.

25 The system of claim 24, wherein said system is adapted to drive substantially simultaneously and asynchronously additional voltage signals onto the respective voltage signal storage elements so as to refresh the stored voltage signals.

Application Serial Number 08/993104

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BOARD OF PATENT APPEALS AND INTERFERENCES

DESIGNATION OF PANEL

Pursuant to (1) the Commissioner's authority to designate the members of the Board of Patent Appeals and Interferences to hear cases before the Board (35 U.S.C. 7(b)), and (2) Commissioner Lehman's memorandum dated May 1, 1994 (delegating to the Chief Administrative Patent Judge the responsibility of designating members to hear cases before the Board), it is ORDERED that the panel of the Board of Patent Appeals and Interferences designated to hear this case shall consist of the following members of the Board:

☑ On Brief ☐ Heard ☐ Redesignation ☐ Expanded Panel, see addendum.

1. Judge Blankenship
2. Judge Hairston ~~Thomas~~
3. Judge Thomas

Bruce H. Stoner, Jr.
BRUCE H. STONER, JR.
Chief Administrative Patent Judge

Date of Hearing: _____